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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,073	01/23/2001	William Frederick Sauber	16356.573 (DC-02636)	2498

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HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202

EXAMINER

NGUYEN, HAU H

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 02/11/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/768,073

Applicant(s)

SAUBER, WILLIAM FREDERICK

Examiner

Hau H Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 2, 3, 5, 7, 8, 11, 12, 14, 16, 17, 19 and 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4, 6, 9, 10, 13, 15, 18 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6, 9, 10, 15, 18, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Zenda (U.S. Patent No. 5,559,525).

Referring to claims 1, 9, 10, 18, and 21, Zenda teach a portable computer having a first graphics subsystem for outputting data to be displayed and a flat panel display unit means for displaying the data supplied from the first graphics subsystem; a second graphics subsystem to be externally connected to the portable computer, for supplying data to be displayed on the flat panel display unit means, to the portable computer; connectors for connecting the second graphics subsystem to the portable computer (col. 2, lines 64-67, and col. 3, lines 1-8). With reference to Fig. 3A, Zenda teaches the first display controller 87 and the RAMDAC 93 constitute a first graphics subsystem (built-in graphics subsystem) (chipset) (see col. 8, lines 12-14). As shown in Fig. 3A, an LCD display board comprising a second display controller 109 is connected to the chipset. The system further comprises a first display device 91, and a second display device 107. Zenda further teaches the selector 113 is connected to the first display controller 87 by the feature connector 103, and to the color LCD controller 95 by the Z connector 105. As illustrated in FIG. 7, the selector 113 (a switching circuit), in response to the changeover signal 115 supplied from the second display controller 109, selects (1) either the

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digital color data supplied from the RAMDAC 111 or the digital color data supplied from the second display controller 109, (2) either the analog video signals supplied from the RAMDAC 111 or the analog video signals from the second display controller 109, and (3) either the control signals coming from the first display controller 87 or the control signals transmitted from the second display controller 109. The selector 113 outputs the selected digital color data and analog video signals (col. 9, lines 27-40).

In regard to claims 6 and 15, as shown in Fig. 1A and 1B, Zenda teaches the system includes a central processing unit (CPU) 57 for controlling the entire system of the computer. Zenda further teach the ZENSEN signal and the enable signal are set by, for example, the software in the register 110 and 116, respectively. More specifically, an initializing routine for initializing the display board is executed after the portable computer is turned on and the selector outputs a correct control signal after the completion of the initializing routine. At this moment, the active low level signals are set to the registers 110 and 116 by a program (col. 10, lines 11-23). Thus, the registers 110 and 116 (system memory) stores a program to control the selector, which in turn, controls the signals to respective display device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zenda (U.S. Patent No. 5,559,525) in view of Behrbaum et al. (U.S. Patent No. 6,326,973).

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Referring to claims 4 and 13, as cited above, Zenda teaches all the limitations of claims 4 and 13, except for the chip set includes an AGP port.

However, Behrbaum et al. teach a computer system using at least one accelerated graphics port (AGP) with at least two core logic chip sets, and more particularly, in allocating AGP/GART memory from the system memory local to the AGP device (col. 1, lines 26-30). As shown in FIG. 4, the computer system 400 has two core logic units 404a and 404b (chip sets). A graphics controller 410 is connected to the AGP bus 413, which, in turn, is connected to the AGP request and reply queues 411 that link the AGP bus 413 to the host bus 403 and the first memory controller 464a (col. 10, lines 7-10, and 14-18).

Therefore, it would have been obvious to one skilled in the art to utilize the method of incorporating an accelerated graphics port to the chip sets as taught by Behrbaum et al. in combination with the teachings as taught by Zenda in order to obtain a low-cost and high speed access to graphics data stored in memory (col. 2, lines 54-61).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

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or faxed to:

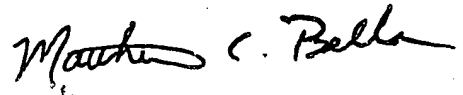
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding
should be directed to the Technology Center 2600 Customer Service Office whose
telephone number is (703) 306-0377.

H. Nguyen

02/05/2004



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600